

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP72312_16M_A

REVISION : 0.1(WEB)

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正基科技股份有限公司



AP72312_16M_A Data Sheet

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Revision

Revision	Date	Description	Revised By
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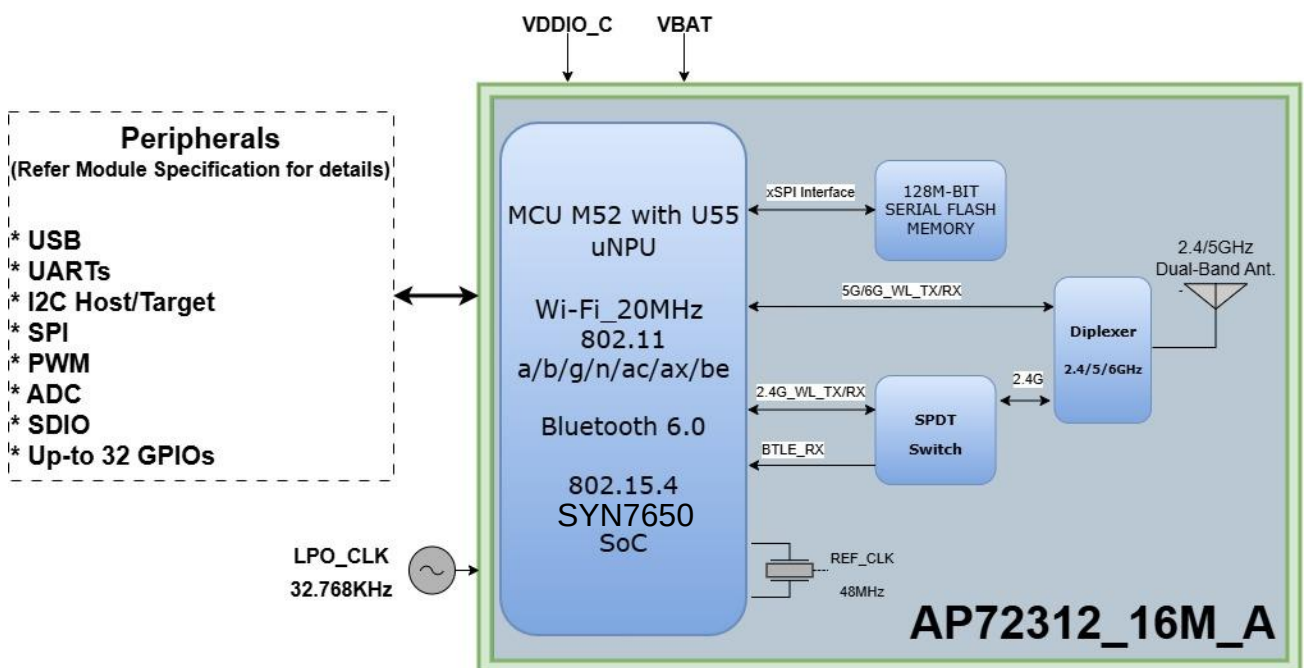
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1. Introduction

1.1 Overview

The AMPAK Technology® AP72312_16M_A is a WLAN (Wi-Fi 7), Bluetooth (6.0), Thread and MCU combination chip with edge AI enabled. It is defined to support two modes of operation, independent master- and slave-mode. In slave mode, the host is the master which is responsible for AP72312_16M_A programming and to fulfill all the requirements for boot and guidance to control the operating modes and features. In master mode, AP72312_16M_A is independent and self-sufficient to boot and operate without any support from external host.

The Ampak AP72312_16M_A smart AIoT device includes an integrated general purpose MCU ARM M52 200-MHz Helium DSP with U55 uNPU 50 GOPS @ 200 MHz, 2.4/5/6 GHz IEEE802.11 a/b/g/n/ac/ax/be MAC/baseband/radio and Bluetooth 6.0 and 802.15.4 Thread.



1.2 Product Features

MCU subsystem

- Arm MCU: Cortex-M52
- Arm NPU: Ethos-U55
- SSE-300–based subsystem interconnect
- Antifuse OTP: 32 Kb
- Frequency up to 200 MHz
- PSA Level 3 security
- Class B safety compliance
- Power modes to support sleep and low-voltage retention
- Independent ON/OFF of WLAN, BT and MCU

Memory

- MCU:
 - SRAM: 1 MB
 - Tightly Coupled Memory (TCM): ITCM 128 KB, DTCM 128 KB
- Serial Flash memory
 - 128M-bit / 16M-byte

Peripherals

- USB, UARTs, I2C Host/Target, SPI, PWM, ADC, SDIO
- Up-to 32 GPIOs (max.)

Security

- Fully firewalled secure CPU
- Secure boot with ECC digital signature verification
- On-module 32 Kb antifuse OTP
- True random number generator
- Hardware accelerators for AES, RSA, SHA, ECC and HASH
- Secure Island SynaPROT support
- PSA Certified™ Level 3 RoT component
- Secure access for Arm Cortex®-M52
- Anti-tamper protection
- Anti-rollback protection and certificate invalidation mechanisms
- Firmware encryption and AES-accelerated secure boot
- TZC/MPC/PPC-based memory isolation for WLAN/BT subsystems

IEEE 802.11 Key Features

- Wi-Fi 7 compliant. IEEE 802.11ax and 802.11be support
- Supports single spatial stream with PHY rate up to 114.7 Mbps.
- 20 MHz channels and up to 256-QAM support for 2.4 GHz, 5 GHz and 6 GHz bands.
- Lead Free design which is compliant with ROHS requirements.
- Supports a standard SDIO v3.0 (4-bit and 1-bit) host interface that is backward compatible with SDIO v2.0.
- Full compatibility with IEEE 802.11a/b/g/n/ac legacy protocols with enhanced performance.

Bluetooth Key Features

- BT Core Specification Version 6.0, including the following support:
 - LE power control
 - LE enhanced connection update
 - LE channel classification
 - Bluetooth BR/EDR
- Bluetooth Class 1 or Class 2 TX operation.
- Bluetooth dedicated 2.4 GHz RF RX input port. Excellent sensitivity and low power are achieved
- Adaptive frequency hopping (AFH) to reduce radio frequency interference.
- Support for Bluetooth Channel Sounding.

IEEE 802.15.4/Thread Key Feature

- Support IEEE 802.15.4/Thread that can act as Border Router.
- Supports Thread V1.3 and Zigbee 3.0 RCP model.

2. General Specification

2.1 General Specification

Model Name	AP72312_16M_A
Product Description	AI-native Connected MCU 1T1R 802.11 a/b/g/n/ac/ax/be Wi-Fi 7 + Bluetooth 6.0
Dimension	L x W : 23 x 35 (typical) mm , H : 2.6(max) mm
WiFi Interface	Supports a standard SDIO v3.0 (4-bit and 1-bit) host interface that is backward compatible with SDIO v2.0
Bluetooth Interface	Host Controller Interface (HCI) using a high-speed UART interface
Operating temperature	-30°C to 85°C (Note)
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.3V < VBAT < 4.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.0	V
VDDIO	Digital/Bluetooth/ I/O Voltage	-0.5	2.07	V

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1.5	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.3	-	4.8	V
VDDIO	1.62	1.8	1.98	V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIH = Input high voltage	$0.65 \times \text{VDDIO}$	NA	V
VIL = Input low voltage	NA	$0.4 \times \text{VDDIO}$	V
VOH = Output high voltage @ 2mA	$\text{VDDIO} - 0.4$	NA	V
VOL = Output low voltage @ 2mA	NA	0.4	V

Programmable 2mA to 16mA drive strength. Default is 10mA.

3. Wi-Fi RF Specification(TBD)

3.1 2.4GHz RF Specification(TBD)

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp=25°C

Feature		Description			
WLAN Standard		IEEE 802.11 b/g/n/ax & Wi-Fi compliant			
Frequency Range		2400 MHz ~ 2483.5 MHz (2.4GHz ISM Band)			
Number of Channels		2400 MHz ~ 2483.5 MHz : Ch1 ~ Ch13			
Modulation		802.11b : DQPSK 、DBPSK 、CCK 802.11g/n : OFDM /64-QAM 、16-QAM 、QPSK 、BPSK 802.11ax : OFDMA /256-QAM 、64-QAM 、16-QAM 、QPSK 、BPSK			
Output Power, tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6 、 9Mbps	12 、 18Mbps	24Mbps	36Mbps	48Mbps
	19	19	18	18	17
	54Mbps				
	17				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	18.5	18.5	18	17	16
	MCS7				
	16				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	18.5	18.5	18	17	16
	HE7	HE8	HE9		
	16	15.5	15		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB				
CCK modulation PER $\leq 8\%$ 、 OFDM modulation PER $\leq 10\%$				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-98		
	2Mbps	-94		
	5.5Mbps	-92		
	11Mbps	-88		

802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-82
	9Mbps	-88	36Mbps	-79
	12Mbps	-86	48Mbps	-76
	18Mbps	-84	54Mbps	-74
802.11n 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-78
	MCS1	-88	MCS5	-76
	MCS2	-85	MCS6	-75
	MCS3	-81	MCS7	-73
802.11ax 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-92	HE6	-76
	HE1	-89	HE7	-74
	HE2	-86	HE8	-72
	HE3	-82	HE9	-70.5
	HE4	-79		
	HE5	-77		
Maximum Input Level	802.11b: -10 dBm			
	802.11g/n/ax: -20 dBm			

3.2 5GHz RF Specification(TBD)

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp=25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac/ax & Wi-Fi compliant			
Frequency Range		5150~5350MHz 、 5470~5725MHz 、 5745~5850MHz （5GHz UNII Band）			
Number of Channels		5150~5350MHz ： Ch36 ~ Ch64 5470~5725MHz ： Ch100 ~ Ch144 5745~5850MHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ax ： OFDMA /1024-QAM 、 256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power, tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	15	15	15	15
	5470~5725	15.5	15.5	15.5	15.5
	5745~5850	15.5	15.5	15.5	15.5
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	15	14.5		
	5470~5725	15.5	15		
	5745~5850	15.5	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	14.5	15	15	15
	5470~5725	15.5	15.5	15.5	15.5
	5745~5850	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	14.5	13.5		
	5470~5725	15	14		
	5745~5850	15	14		

802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	14.5	15	15	15
	5470~5725	15.5	15.5	15.5	15.5
	5745~5850	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	14.5	13.5	12	
	5470~5725	15	14	12.5	
	5745~5850	15	14	12.5	
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	14.5	15	15	15
	5470~5725	15.5	15.5	15.5	15.5
	5745~5850	15.5	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	14.5	13.5	12	11
	5470~5725	15	14	12.5	11.5
	5745~5850	15	14	12.5	11.5
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB CCK modulation PER $\leq 8\%$、OFDM modulation PER $\leq 10\%$					
802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	6Mbps	-90	24Mbps	-83	
	9Mbps	-89	36Mbps	-79	
	12Mbps	-88	48Mbps	-74	
	18Mbps	-86	54Mbps	-73	
802.11n 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	MCS0	-90	MCS4	-79	
	MCS1	-88	MCS5	-75	
	MCS2	-86	MCS6	-72	
	MCS3	-83	MCS7	-71	
802.11ac 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	MCS0	-90	MCS5	-75	
	MCS1	-88	MCS6	-72	

	MCS2	-86	MCS7	-71
	MCS3	-83	MCS8	-67
	MCS4	-79		
802.11ax 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-72
	HE1	-88	HE7	-71
	HE2	-86	HE8	-67
	HE3	-83	HE9	-64
	HE4	-79		
	HE5	-75		
Maximum Input Level	802.11a/n/ac/ax: -30 dBm			

3.3 6GHz RF Specification(TBD)

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp=25°C

Feature		Description			
WLAN Standard		IEEE 802.11ax & Wi-Fi compliant			
Frequency Range		5925~7125MHz (6GHz U-NII5, U-NII6, U-NII-7, U-NII-8 Band)			
Number of Channels		5925~6425MHz：6G1 ~ 6G93 6425~6525MHz：6G97 ~ 6G113 6525~6875MHz：6G117~6G181 6875~7125MHz：6G185~6G233			
Modulation		802.11ax：OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 2.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5925~6425	14	14	14	14
	6425~6525	13.5	13.5	13.5	13.5
	6535~6675	13.5	13.5	13.5	13.5
	6695~7125	12	12	12	12
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5925~6425	13.5	12.5	11	10.5
	6425~6525	13.5	12.5	11	10.5
	6535~6675	13.5	12.5	11	10.5
	6695~7125	11.5	10.5	8.5	7.5

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB, OFDM modulation PER $\leq 10\%$					
802.11ax 20MHz	Frequency (MHz)	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	5925~6425	HE0	-89	HE5	-74
		HE1	-86	HE6	-71
		HE2	-84	HE7	-68
		HE3	-83	HE8	-66
		HE4	-77	HE9	-63
	Frequency (MHz)	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6425~6525	HE0	-89	HE5	-74
		HE1	-86	HE6	-71
		HE2	-84	HE7	-68
		HE3	-83	HE8	-66
		HE4	-77	HE9	-63
	Frequency (MHz)	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6525~6875	HE0	-89	HE5	-74
		HE1	-86	HE6	-71
		HE2	-84	HE7	-68
		HE3	-83	HE8	-66
		HE4	-77	HE9	-63
	Frequency (MHz)	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6875~7125	HE0	-86	HE5	-70
		HE1	-82	HE6	-67
		HE2	-80	HE7	-64
		HE3	-79	HE8	-62
		HE4	-73	HE9	-59

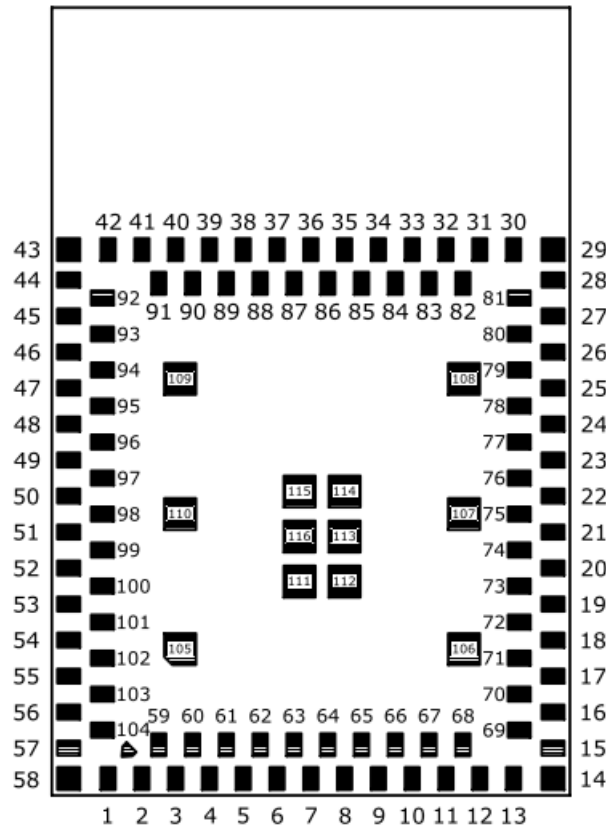
4. Bluetooth Specification(TBD)

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
General Specification	
Bluetooth Standard	BDR、EDR(1Mbps & 2Mbps)、LE(1Mbps)、2LE(2Mbps) LELR(125Kbps)、LELR(500Kbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic、40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power, tolerance ± 2.5 dB	
	CL1 (dBm)
BDR Output Power	7
EDR Output Power	6
BLE Output Power	7
Sensitivity, tolerance ± 2.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-87 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-89 dBm
Sensitivity @ BER=0.01%for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-90 dBm
Sensitivity @ PER=30.8% for LELR (125Kbps)	-100 dBm
Sensitivity @ PER=30.8% for LELR (500Kbps)	-95 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

<TOP VIEW>



NO	Name	Type	Description
1	MCU_GPIO10_XSPI_CS1	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
2	USB_VBUS (5V_IN)	P	USB 2.0 VBUS power input (+5V)
3	GND	P	Ground connections
4	USB_DP	I/O	USB 2.0 Data Positive
5	USB_DN	I/O	USB 2.0 Data Minus
6	GND	P	Ground connections
7	GND	P	Ground connections
8	GND	P	Ground connections
9	GND	P	Ground connections
10	VBAT	P	DC supply for VBAT

			Refer to the 2.2.2 Recommended Operating Rating for details.
11	VBAT	P	DC supply for VBAT Refer to the 2.2.2 Recommended Operating Rating for details.
12	GND	P	Ground connections
13	GND	P	Ground connections
14	GND	P	Ground connections
15	CHIP_PAD_REG_ON	I	Power Up (high)/ Shutdown (Low) the module. Power enabled active high and disable active low Refer to the 8. Host Interface for details.
16	MCU_GPIO28	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
17	MCU_GPIO24	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
18	MCU_GPIO22	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
19	GND	P	Ground connections
20	MCU_GPIO15	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
21	MCU_GPIO17	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
22	MCU_GPIO19	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
23	GND	P	Ground connections
24	GPADC_IN1	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
25	GPADC_IN2	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
26	GPADC_IN5	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
27	GPADC_IN7	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
28	GP_DAC_OUT	O	General-Purpose Digital-to-Analog Converter output.
29	GND	P	Ground connections
30	GND	P	Ground connections
31	GND	P	Ground connections
32	GND	P	Ground connections

33	GND	P	Ground connections
34	GND	P	Ground connections
35	GND	P	Ground connections
36	GND	P	Ground connections
37	GND	P	Ground connections
38	GND	P	Ground connections
39	GND	P	Ground connections
40	GND	P	Ground connections
41	GND	P	Ground connections
42	GND	P	Ground connections
43	GND	P	Ground connections
44	GND	P	Ground connections
45	GND	P	Ground connections
46	RF_SW_CTRL_1	I/O	GPIOs : MCU_GPIO_27, For details, please refer to the GPIO Alternative Signal Functions.
47	RF_SW_CTRL_3	I/O	GPIOs : MCU_GPIO_27, For details, please refer to the GPIO Alternative Signal Functions.
48	MCU_GPIO21/ STRAPO (PLL BYPASS)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions. Refer to the Boot Option settings for details.
49	MCU_GPIO13	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
50	GND	P	Ground connections
51	LPO_IN	I	External 32.768 kHz Low-Power Oscillator Input
52	GND	P	Ground connections
53	MCU_GPIO5	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
54	MCU_GPIO7	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
55	MCU_GPIO_12	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
56	GND	P	Ground connections
57	VDDIO_C	P	DC supply voltage for digital I/O Refer to the 2.2.2 Recommended Operating Rating for details.
58	GND	P	Ground connections
59	MCU_GPIO3/STRAP8 (DAP SEL)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.

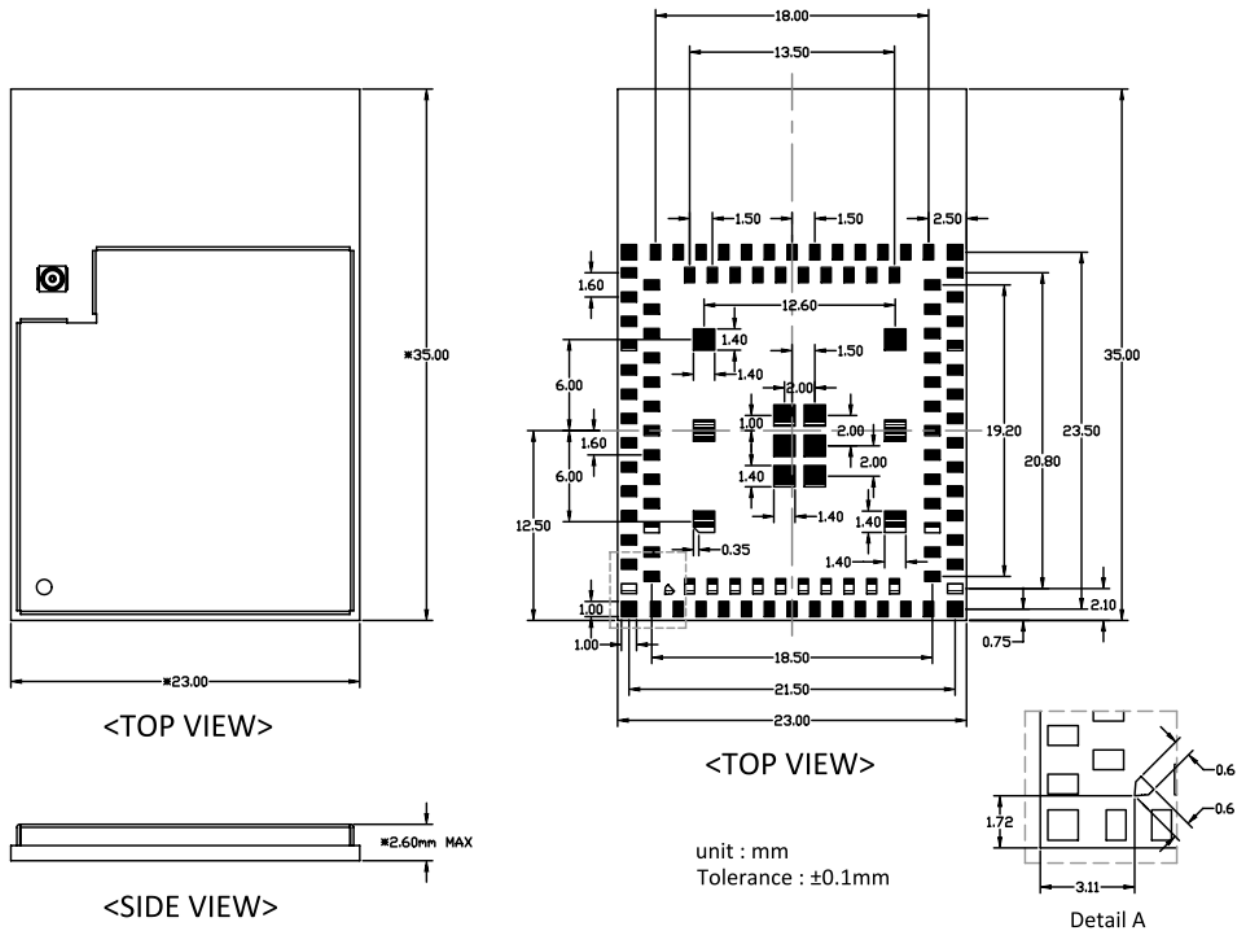
			Refer to the Boot Option settings for details.
60	MCU_GPIO4/STRAP9(DAP SEL)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions. Refer to the Boot Option settings for details.
61	USB_USB0ID	—	This pin is reserved. (Floating)
62	GND	P	Ground connections
63	GND	P	Ground connections
64	GND	P	Ground connections
65	GND	P	Ground connections
66	GND	P	Ground connections
67	VBAT	P	DC supply for VBAT Refer to the 2.2.2 Recommended Operating Rating for details.
68	GND	P	Ground connections
69	MCU_GPIO29	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
70	MCU_ATE_MODE_RESETN	I	This pin is reserved. An external 10 kΩ pull-up resistor is required.
71	MCU_GPIO25	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
72	MCU_GPIO23	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
73	MCU_GPIO14	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
74	MCU_GPIO16	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
75	MCU_GPIO18	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
76	GND	P	Ground connections
77	GPADC_IN0	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
78	GPADC_IN3	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
79	GPADC_IN4	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
80	GPADC_IN6	I	Analog input channel of the General-Purpose ADC. please refer to the GPIO Alternative Signal Functions.
81	AU_DAC_OUT	O	This pin is reserved. (Floating)

82	GND	P	Ground connections
83	GND	P	Ground connections
84	GND	P	Ground connections
85	GND	P	Ground connections
86	GND	P	Ground connections
87	GND	P	Ground connections
88	GND	P	Ground connections
89	GND	P	Ground connections
90	GND	P	Ground connections
91	GND	P	Ground connections
92	GND	P	Ground connections
93	GND	P	Ground connections
94	RF_SW_CTRL_0	I/O	GPIOs : MCU_GPIO_26, For details, please refer to the GPIO Alternative Signal Functions.
95	RF_SW_CTRL_4	I/O	GPIOs : MCU_GPIO_20, For details, please refer to the GPIO Alternative Signal Functions.
96	MCU_GPIO20/STRAP7 (DVT MODE)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions. Refer to the Boot Option settings for details.
97	MCU_GPIO30/STRAP2(BOOT)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions. Refer to the Boot Option settings for details.
98	MCU_GPIO31/STRAP1(BOOT)	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions. Refer to the Boot Option settings for details.
99	MCU_GPIO0	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
100	MCU_GPIO6	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
101	GND	P	Ground connections
102	MCU_GPIO8	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
103	MCU_GPIO9/XSPI_CS0	I/O	GPIOs, For details, please refer to the GPIO Alternative Signal Functions.
104	VDDIO_C	P	DC supply voltage for digital I/O, Refer to the 2.2.2 Recommended Operating Rating for details.
105	GND	P	Ground connections
106	GND	P	Ground connections

107	GND	P	Ground connections
108	GND	P	Ground connections
109	GND	P	Ground connections
110	GND	P	Ground connections
111	GND	P	Ground connections
112	GND	P	Ground connections
113	GND	P	Ground connections
114	GND	P	Ground connections
115	GND	P	Ground connections
116	GND	P	Ground connections

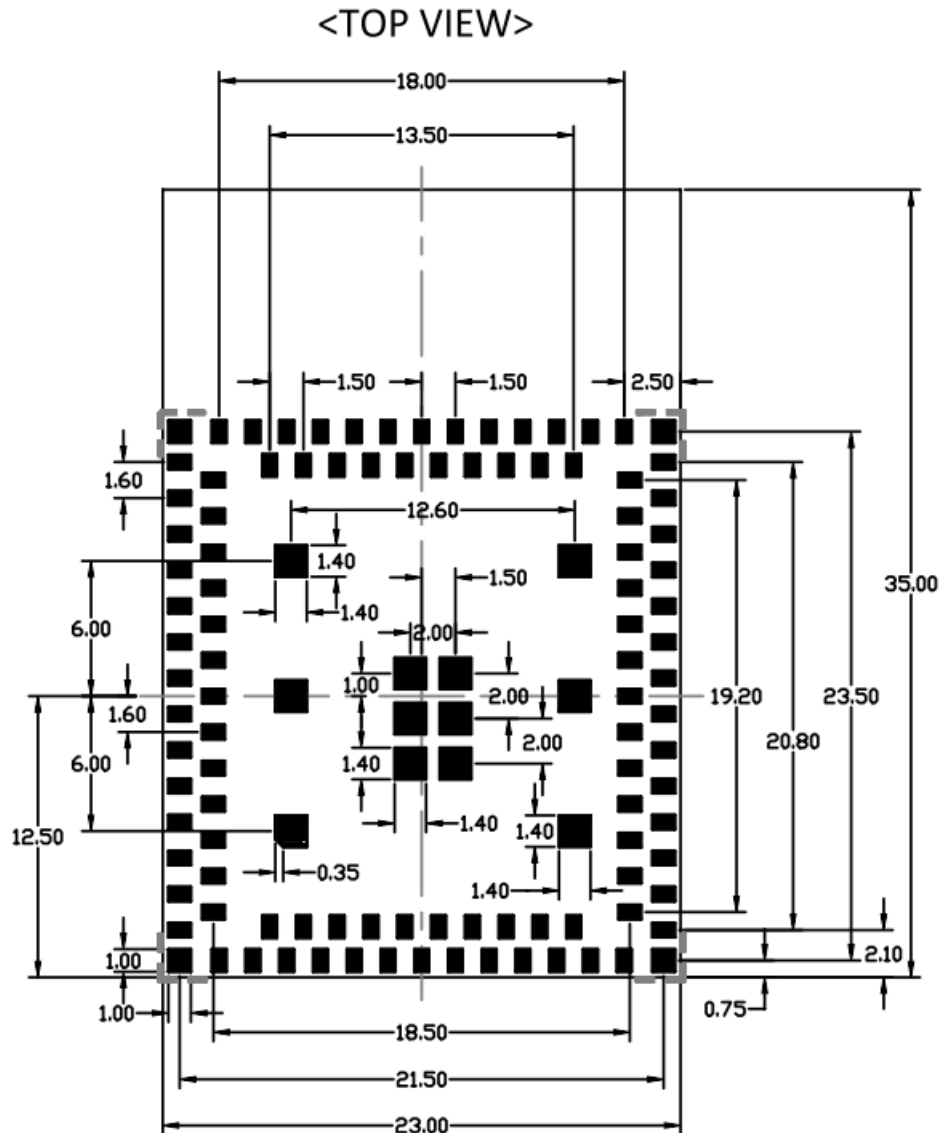
6. Dimensions

6.1 Module Physical Dimensions



PHYSICAL DIMENSIONS

6.2 Recommended footprint



- Solder paste layer design is generally the same as recommended footprint.
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial. In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.

7. External clock reference

External 32.768 kHz Low-Power Oscillator

The AP72312_16M_A uses a secondary low-frequency clock for low-power mode timing. Either the internal low precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ($\pm 30\%$) over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power-save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock which meets the requirements listed in the following table.

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8 $\pm$ 0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

8. Host Interface (TBD)

8.1 Reset and Regulator Control Signals Sequencing

Single control signals, CHIP_REG_ON is used to power-up the regulators and take the respective sections out of reset as per power-up sequence. All regulators are powered down only when control signals are de-asserted.

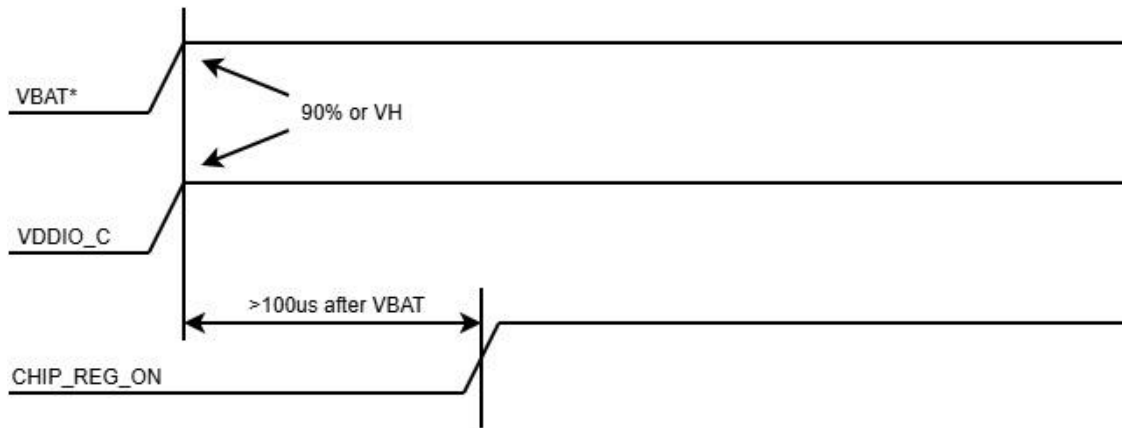
- **CHIP_PAD_REG_ON:** In stand-alone systems (no external host), the module operates as the host and can enter shutdown when not needed using CHIP_PAD_REG_ON. The device restores operation through the CHIP_PAD_REG_ON pin, which controls power-up and reactivation of internal circuitry. In systems with an external host, shutdown is initiated by the host while the module's I/O domain stays powered to avoid loading shared interfaces. In this mode, power-up remains controlled by the CHIP_PAD_REG_ON pin, while wake-up events are triggered by a host-provided GPIO, enabling precise host-managed power sequencing and minimizing system power consumption. When the module is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down. The module integrate PMU has an under voltage lockout (ULVO). When it detects either VBAT < 2.23V or VDDIO < 1.52V, it will shut down the PMU (Module).

8.2 Start-Up Sequences

The AP72312_16M_A module has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDIO_C have both passed the POR threshold. Wait at least 150 ms after VDDIO_C are available before initiating PCIe accesses.

The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 μ s/V.

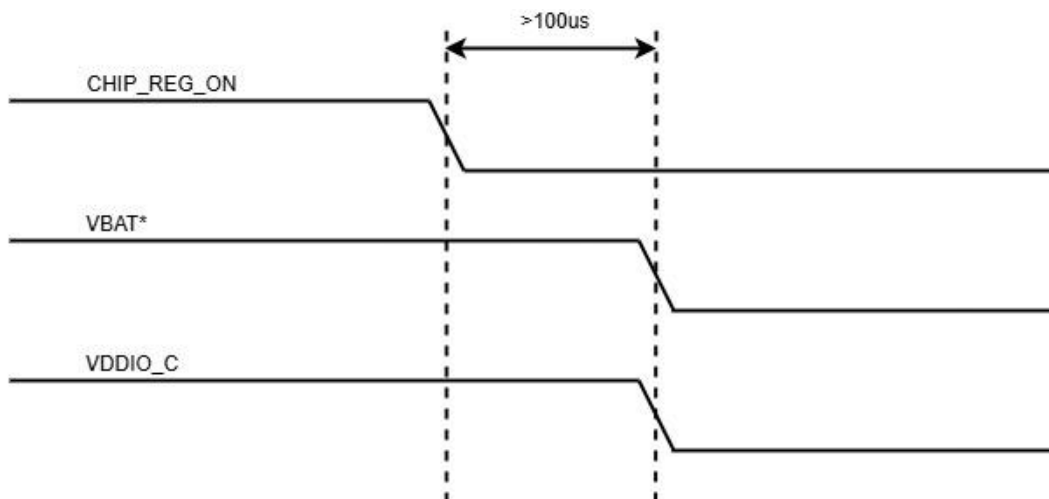
Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.



***Notes**

1. The VBAT and VDDIO_C 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO_C. VDDIO_C should not be present first or be held high before VBAT is high.

WLNA=ON ; Bluetooth=ON



***Notes**

1. The VBAT and VDDIO_C 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO_C. VDDIO_C should not be present first or be held high before VBAT is high.

WLNA=OFF ; Bluetooth=OFF

9. Module Built-in of MCU Interface (TBD)

9.1 Overview

The AP72312_16M_A module integrates an on-chip Arm Cortex-M52 CPU to run application software, along with an embedded hardware cryptographic accelerator to meet system security requirements. This AP72312_16M_A module supports both on-module host and off-module host operating models.

The module built-in of MCU subsystem consists of multiple components, including a dedicated Security Island (Ampak) that is responsible for key storage and security services for the rest of the system. The MCU subsystem also includes a cryptographic accelerator, on-chip memory, and OTP storage.

The module built-in of MCU subsystem include rich set of peripheral and accelerators:

- USB 2.0 dual-role up to 480Mbps (LS/FS/HS)
- UARTs with flow control and for debug
- I2C Host and Target
- SPI Host supports up to 25MHz and Target up to 25MHz
- PWMs supporting Motor Control & LED Brightness features
- PDM interface support 2 Digital Mics
- I2S with simultaneous RX/TX
- GPIOs
- SDIO
- ADC: 8-channel General Purpose ADC (Can be converted to GPIO if ADC channels is not used)
- General purpose DAC

9.2 USB2.0

The USB 2.0 OTG controller performs as a standard Hi-Speed, Dual-Role Device (DRD), operating as either a USB 2.0 Hi-Speed compliant peripheral, or Hi-Speed USB 2.0 host.

The USB2.0 supports the following features:

- Fully compliant with USB specifications Rev 2.0, 1.1 & OTG
- Supports 480Mbps (HS), 12Mbps (FS)& 1.5Mbps (LS) serial data transmission
- Support Serial Mode For FS (12Mbps) and LS (1.5Mbps) Modes
- Built-in I/O and ESD structure
- On-die self-calibrated HS/FS/LS termination
- 24/20MHz external crystal or on chip reference clock with Integrated phase-locked loop (PLL)

9.3 SDIO V3.0 Interface Description

The module built-in of MCU provides support for SDIO version 3.0 at 1.8V signaling, including the new UHS-I modes:

DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes.

SDR12: SDR up to 25 MHz.

SDR25: SDR up to 50 MHz.

SDR50: SDR up to 100 MHz.

SDR104: SDR up to 150 MHz.

DDR50: DDR up to 50 MHz.

Note:

The module is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also can map the interrupt signal to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options.

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Note:

Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

9.4 GPIOs Interface Description

The AP72312_16M_A module has 32 general-purpose I/O (GPIO) pins in the MCU section that can be used to connect to various external devices.

Upon power-up and reset, these pins become tri-stated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions by configuring pin multiplexing mode.

9.5 I2C Interface Description

The I2C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL).

These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as hosts or targets when performing data transfers.

The feature set include

- Three speeds:
 - ✧ Standard mode (0 to 100 Kb/s)
 - ✧ Fast mode (
 - ✧ ≤ 400 Kb/s) or fast mode plus (≤ 1000 kb/s)
- High-speed mode (≤ 3.4 Mb/s)
- 7- or 10-bit addressing
- Bulk transmit mode
- Ultra-Fast mode support
- I2C supports host or target operation.

9.6 UART Interface Description

Universal Asynchronous Receiver/Transmitter (UART) modeled after the industry-standard 16550. UART is used for serial communication with peripheral. UART supports configurable character length, baud rate, parity generation/checking. There are three instances of UART with support for full flow control.

Feature set include following

- 9-bit serial data support
- False start bit detection
- Programmable fractional baud rate support
- Functionality based on the 16550 industry standard
 - ✧ Programmable character properties, such as:
 - Number of data bits per character (5-8)
 - Optional parity bit (with odd, even select or Stick Parity)
 - Number of stop bits (1, 1.5 or 2)
 - ✧ Line break generation and detection
 - ✧ DMA signaling with two programmable mode
 - ✧ Prioritized interrupt identification

9.7 SPI Interface Description

SPI peripheral can be configured in one of two modes of operations: as a serial host or a serial target. The SPI can connect to any serial-host or serial-target peripheral device using one of the following interfaces:

- Motorola Serial Peripheral Interface (SPI)
- Texas Instruments Serial Protocol (SSP)
- National Semiconductor Microwire

9.8 PDM Interface Description

The pulse density modulation (PDM) enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (left and right) data input. Data is transferred directly to RAM buffers using DMA.

Features for PDM include the following:

- Up to two PDM microphones configured as a left/right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- HW decimation filters

DMIC stream is decimated from the digital microphone rate (512KHz to 3.072MHz) to a recording rate of from 8KHz to 192KHZ. Within the record decimation path, the sequence of filters is a function of the input (DMIC) and output (record) sample rates.

9.9 PWM Interface Description

The Timer, Counter, and Pulse Width Modulator (TCPWM) block implements a 16- or 32-bit timer, counter, pulse width modulator (PWM), pseudo random PWM, shift register, and quadrature decoder functionality. TCPWM supports up to up to 6 counters. The counter can be used to measure the period and pulse width of an input signal (timer), find the number of times an event occurs (counter), generate PWM signals, or decode quadrature signals.

- Each counter can run in one of seven function modes:
 - ✧ Timer-counter with compare
 - ✧ Timer-counter with capture
 - ✧ Quadrature decoding
 - ✧ Pulse width modulation/stepper motor control (SMC) for pointer instruments
 - ✧ PWM with dead time/three-phase motor control (Brushless-DC, BLDC)
 - ✧ Pseudo-random PWM
 - ✧ Shift register mode
- 16-bit or 32-bit counters (configurable and project specific)

- Up, down, and up/down counting modes
- Clock prescaling (division by 1, 2, 4, ... 64, 128)

9.10 I2S Interface Description

The Integrated Inter-IC Sound Bus (I2S) is a serial bus interface standard used for connecting digital audio devices together.

I2S feature set include:

- Philips/Sony/Right Justified/Intel/PCM/TDM mode.
- Host and target mode.
- Sharing of the SCK & WS signal between transmitter and receiver.
- Programmable assertion duration and frame length for WS signal in host mode.
- Programmable polarity of first frame for WS signal in host mode.
- Programmable sample size.
- Minimum slot of 1 cycle.
- Either SCK edge for SD signal.
- Programmable 'left then right' or 'right then left' order.
- Programmable bit order, MSB or LSB.
- Programmable polarity for WS signal.
- Any sample rate.

9.11 ADC Interface Description

ADC is a Successive Approximation Register (SAR) architecture. The maximum resolution is 12 bits, which can achieve 1.536 millions samples per second (MSPS). This ADC support input MUX which can select the up to simultaneous 8 inputs from external pins. This ADC need configuration from CPU, later it can operate independently. The ADC can be clocked at different speeds. This ADC support internal calibration mode to correct for any irregularity due to process/temperature variation.

9.12 DAC Interface Description

DAC support 10 bit resolution. DAC support following mode of operation

- Single conversion mode. This mode provide fixed reference voltage at DAC output.
- Continuous conversion mode. Continuous stream of data is provided to DAC using internal DMA. DAC generate varying output as governed by input data stream
- Comparator mode. Input value is compared against the specified reference and the interrupt is generated is threshold is crossed.

10. Security Overview

The device implements a multi-processor security architecture built around a dedicated Secure Island Processor (SynaPROT Root of Trust), providing the foundation for all secure operations.

At power-up, the Secure Island powers on first and executes immutable ROM-based Root of Trust (RoT) code.

This stage authenticates and loads the Secure Processor Kernel (SPK) using ECC digital signature verification.

Once the SPK is validated and running, it authenticates the module built-in of MCU bootloader image before releasing control to the module built-in of MCU domain.

The module built-in of MCU then acts as the orchestrator for higher-level functions and, as required, initiates the bring up of the WLAN and Bluetooth subsystems. Each subsystem includes its own ROM-based bootloader that enforces secure boot validation with the assistance of the Secure Island.

The module built-in of all image authentication uses Tamper proof hardware-accelerated AES and ECC engines located in the Secure Island.

The module built-in of firmware images for WLAN and Bluetooth are encrypted and verified prior to execution, with additional protection through anti-rollback and certificate invalidation mechanisms. Subsystem memory regions are isolated using TrustZone Controller (TZC) for WLAN and Memory/Peripheral Protection Controllers (MPC/PPC) for Bluetooth, ensuring strict domain separation and preventing unauthorized access.

This layered security model provides a hardware-anchored chain of trust spanning all processors, from power-on reset through subsystem firmware validation, ensuring robust protection against unauthorized code execution and firmware tampering.

11. NPU Description (TBD)

The Neural Processing Unit (NPU) improves the inference performance of neural networks. The NPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN). The NPU supports 8-bit weights.

The NPU includes a Direct Memory Access (DMA) controller that can read and write to external memory. When the NPU performs inferences, the DMA controller reads the neural network description. This description contains:

- The command stream
- Network weights
- Bias information
- Scale information

The DMA controller also transfers the Input Feature Maps (IFMs) and Output Feature Maps (OFMs) and NPU-private intermediate data that is also held in system memory.

During runtime, TensorFlow Lite (TFL) loads the flatbuf file, in which the OpenVINO Compiler has created an Ethos™-U55 command stream for each custom operator. The driver gives a pointer to this command stream so that the NPU hardware can execute it. This means that the entire network can be a single operator that is run fully on the Ethos™-U55. The NPU reads the data (weights, commands, IFMs, OFMs, bias and scale) autonomously using the DMA.

The NPU uses a working buffer in SRAM for IFMs and OFMs in flight. The OpenVINO Compiler decides the scheduling of this buffer and codes it into the command stream. The NPU uses the DMA to read and write autonomously to this work buffer. The location of the buffer is set at runtime through registers, meaning the coding in the command stream is relative, not absolute

12. Boot Option (TBD)

The module built-in of MCU subsystem support boot from following interfaces

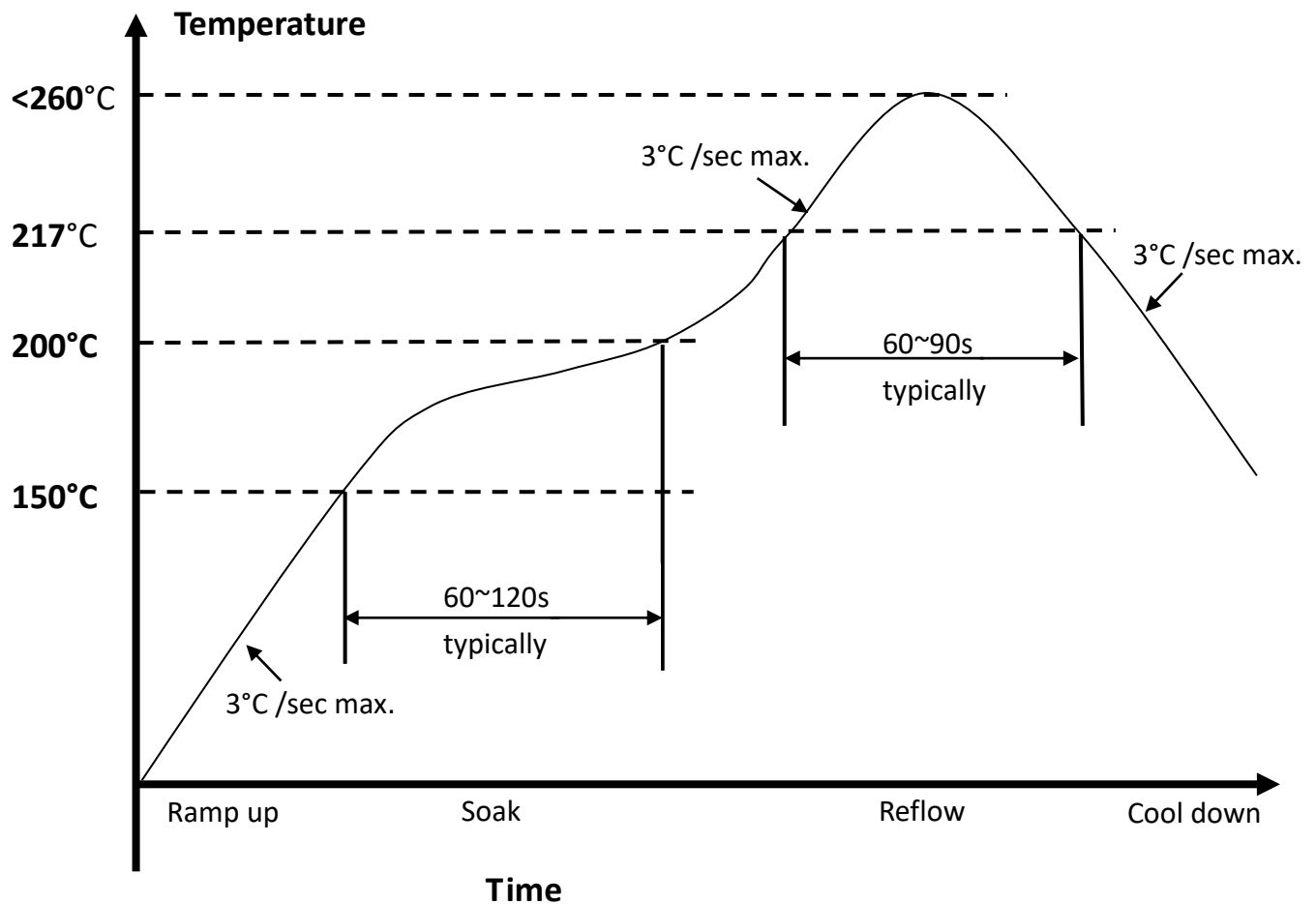
- Flash
- SDIO
- USB2.0
- SPI
- UART

Boot option is selectable using bootstrapping pins.

PIN Name	Strap Name	Description	Default pull
MCU GPIO {30:31}	BOOT	Boot strap to indicate which source need to be used to load the software and M52 code 00: Boot from USB 01: Boot from OSPI 10: Boot from SDIO 11: Boot from other (SPI,I2C,UART)	None
MCU_GPIO21	PLLBYPASS	Boot strap to indicate the PLL Bypass, so the boot ROM won't switch the clock to PLL but continue with RC oscillator clock	Pull Down
MCU_GPIO{4,3}	DAPSEL	Select DAP for M52 00 – Functional pin mux. 11 – MCU DAP selection	Pull Down

13. GPIO Alternative Signal Functions (TBD)

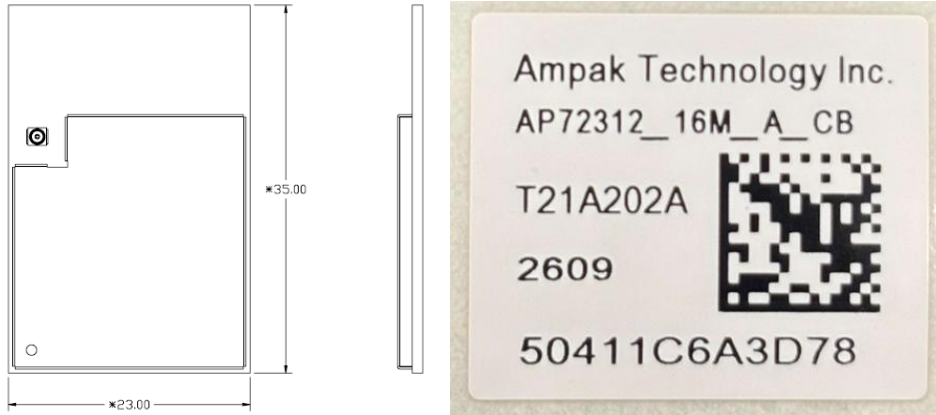
14. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C (Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

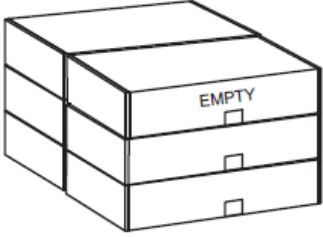
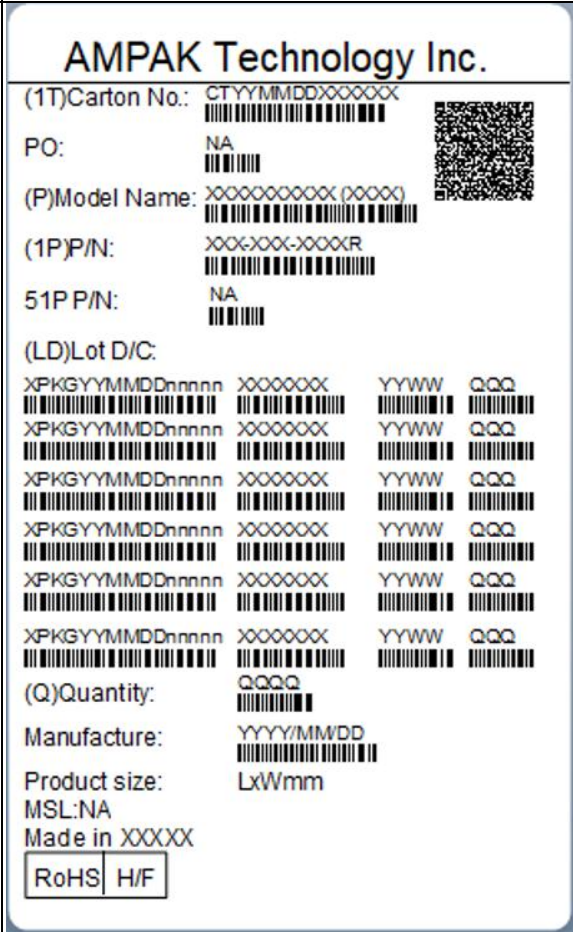
15. Package Information (TBD)

15.1 Module Label



15.2 Packing

Items	Photo	Description
1		IC Tray (Schematic diagram) (For reference only, depend on the quantity of tray packaged.)
2		Inner box (Box) Quantity: QQQ pcs/box (For reference only, depend on the quantity of tray packaged.)
3	(1T)PKG S/N: XPKGYYMMDDnnnn PO: NA (P)Model Name: XXXXXXXXXXX (XXXX) (1P)P/N: XXX-XXX-XXXXR 51P P/N: NA (L)Lot Code: XXXXXXXX (D)Date Code: YYWW (Q)Quantity: QQQQ Product size: LxWmm MSL:NA Made in Taiwan RoHS H/F	Inner box (Box) label The label content includes barcode

4		6 inner boxes per outer box (Carton) Quantity: QQQQ pcs/outer box (Carton) (For reference only, depend on the quantity of tray packaged.)
5		Outer box (Carton) Quantity: QQQQpcs/outer box (Carton) (For reference only, depend on the quantity of tray packaged.)
6		Outer box (Carton) label The label content includes barcode